Journal of Energy Technology

JET Volume 10 (2017) p.p. 35-50
Issue 2, June 2017
Type of article 1.02
www.fe.um.si/en/jet.html

EFFICIENT APPLICATIONS AND ARCHITECTURE OF MODERN DIGITAL SIGNAL PROCESSORS

UČINKOVITE APLIKACIJE IN ARHITEKTURE MODERNIH DIGITALNIH SIGNALNIH PROCESORJEV

Ivana Hartmann Tolić[ℜ], Snježana Rimac-Drlje[1], Željko Hocenski[1]

Keywords: digital signal processor, parallel processing, Harvard processor architecture, evaluation model

Abstract

Digital signal processors have found their roles in various fields of science and technology. With the appearance of problems related to the processing of large quantities of data in real time, it was necessary to develop a system that would execute procedures very rapidly and at low cost. The most common application in real time is the digitization and mathematical processing of audio, video, temperature, and voltage data, etc., resolved using parallel operations. Various producers of digital signal processors have developed processors and evaluation models that enable developers to quickly and efficiently create unique applications in communications and visual systems, biomedicine, meteorology, etc. In this article, the basic performance and architecture of the modern digital signal processor are described in detail with emphasis on the most common applications. A practical example of the use of a digital signal processor for numerical integration is presented. A comparison with commonly used processors is performed to confirm its efficiency..

ℜ Corresponding author: Ivana Hartmann Tolić, J. J. Strossmayer University in Osijek, Faculty of Electrical Engineering, Computer Science and Information Technology in Osijek, Kneza Trpimira 2b, Osijek, Croatia, Tel: +385 31 495 416, e-mail address: ivana.hartmann@etfos.hr

[1] J. J. Strossmayer University in Osijek, Faculty of Electrical Engineering, Computer Science and Information Technology in Osijek, Kneza Trpimira 2b, Osijek, Croatia

Povzetek

Digitalni signalni procesorji se pojavljajo v različnih panogah znanosti in tehnologije. S pojavom problemov, ki zahtevajo procesiranje velikih količin podatkov v realnem času, je bilo potrebno razviti sistem, ki je sposoben izvajati operacije z večjo hitrostjo in nižjimi stroški. Najpogostejše aplikacije v realnem času so digitalizacija, matematično procesiranje avdio in video signala, temperature, napetosti ipd., ki se izvajajo z vzporednimi operacijami. Različni proizvajalci digitalnih signalnih procesorjev so razvili procesorje in ocenjevalne postopke, ki omogočajo razvijalcem hitro in učinkovito ustvarjanje edinstvenih aplikacij na področju telekomunikacij, vizualnih sistemov, biomedicine, meteorologije ipd. V članku je podrobno opisano osnovno delovanje in arhitektura modernih digitalnih signalnih procesorjev s poudarkom na najpogosteje uporabljenih aplikacijah. Predstavljen je praktični primer aplikacije digitalnega signalnega procesorja za numerično integracijo. Za potrditev učinkovitosti je podana primerjava z drugimi pogosto uporabljenimi tipi procesorjev.

1 INTRODUCTION

Digital signal processors (DSP) are used for collecting large amounts of data, which are the subject of mathematical transformations that give very good results in real time systems. Due to their basic characteristics, DSP application vary from practical everyday devices (cell phone, camera, etc.) to medical, military, scientific research and evolutionary models.

The first appearance of the DSP was in the 1970s, and it was first dominant in telecommunications, high-speed modems, military applications and medicine, because these fields could financially support the development of the expensive technology at that time. A group of engineers from Texas Instruments (TI) presented the first commercial DSP whose architecture is the closest to today's DSPs at International Solid-State Circuits Conference (ISSCC) in February 1982. Their first device was the TMS32010 with 5 million instructions per second and with 55,000 transistors, *[1]*. To enter the consumer market, they created a talking and listening doll named Julie, and the TMS320C17 was used for voice recognition. They also wanted to attract more customers and expand into more areas, so they started from the basic knowledge of digital signal processing and observed huge losses of energy; their aim was to reduce it, *[1]*. Nowadays, most of the devices that process graphics and sounds cannot be imagined without a specialized DSP processor.

In this paper, the authors analyse the basic features and architecture of DSPs. The paper is structured as follows: Section 2 presents basic performance and the architecture of DSPs; Section 4 presents the most commonly used applications and algorithms using DSPs; practical implementation is presented on a Texas Instrument evaluation model in Section 4.

2 BASIC PERFORMANCE AND ARCHITECTURE OF THE DSP

A DSP is a microprocessor that has high data flow and can process fast streaming, e.g. multimedia data processing. The execution time of the program using a DSP can be predicted and thus desirable results are guaranteed. It is possible to obtain different behaviour from the system through the reprogramming of the DSP with relevant software, i.e. with decoding algorithm execution, *[2]*. Programs written for regular processors are written in high-level programming languages, but programs for the DSP are more commonly written in an assembly language because of the standard DSP architecture (multiple memory spaces, buses, irregular sets of instructions and highly specialized hardware), *[3]*. A DSP is a microprocessor designed for fast problem solving in digital signal processing, in particular for the rapid execution of arithmetic and logical operations and has the capability of executing one or more parallel multiply-accumulate (MAC) operations in one instruction cycle. The time of the MAC operations execution is not a primary feature of the DSP, but faster MAC operations provide better bandwidth. Due to the latter, two or more MAC units are embedded in modern DSPs. MAC operations are common in DSP applications, and they are used for vector multiplication, digital filters, correlations and Fourier transformations, *[4]*, *[5]*. DSPs are commonly used for real-time processes, and they receive real time signals for audio, video, temperature, pressure or location that have to be digitized and mathematically processed in real time. They are designed for fast execution of the finite impulse response filters (FIR), which are used in digital signal processing. A FIR filter is implemented in real-time and uses circular buffering carried out through the steps listed below. The 14 steps are running parallel on a DSP, unlike on a traditional microprocessor where they are serially executed *[4], [5]*. Because the algorithm has to be executed quickly, internal DSPs architecture allows the execution in one cycle operations of the loop which contains steps 6-12 and they are repeated circularly, *[5]*.

Selecting an adequate digital signal processor is an important but not easy task due to the great number of available processors. It is necessary to consider the following, *[6]*:

- architectural features – when selecting a DSP, it is important to pay attention to on-chip memory, input/output options, RAM etc. because DSPs are not multifunctional
- execution speed – even though there are two basic measurement units of the CPU clock speed (MHz) and the number of instructions processed per second that a computer can process (MIPS), due to the various numbers of multiple operations of different DSPs, an alternative measure is based on a speed performance benchmark algorithm.
- type of the arithmetic – although most of the PDSPs use fixed-point arithmetic, floating point arithmetic is more efficient, more precise and needs less execution time but, because of optimized DSP arithmetic, the speed is approximately equal. For temporarily storing the results of DSP with fixed-point arithmetic, the additional accumulator registers are joined.
- word length – DSP with fixed-point designed for telecommunications uses 16-bit word length and processors intended for high-quality 24-bit word length audio applications. DSP with floating point arithmetic uses the 32-bit word length.

In standard microprocessors, based on Von Neumann architecture, operations are executed sequentially, which commonly results in data flow congestion, as shown in Fig. 1. When aspiring for a faster processor and faster execution of the mathematical instructions in digital signal processing, it is necessary to separate the buses, i.e. use dual bus architecture (separate memory for data and memory for program instructions). This concept of processor is called Harvard architecture, and it is used in most of the modern DSPs; it is presented in Fig. 1, *[5]*–*[7]*. The use of two separate memory buses assures simultaneous data and instruction flow and provides the ability for fetching more options in every instruction cycle, *[8]*.

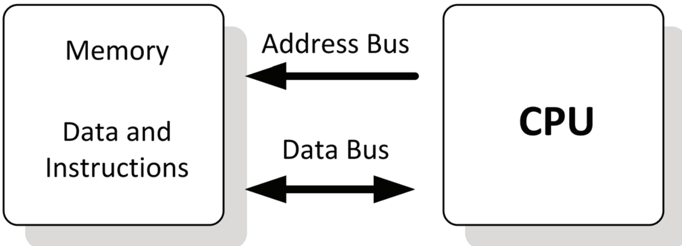

Figure. 1. Von Neumann processor architecture

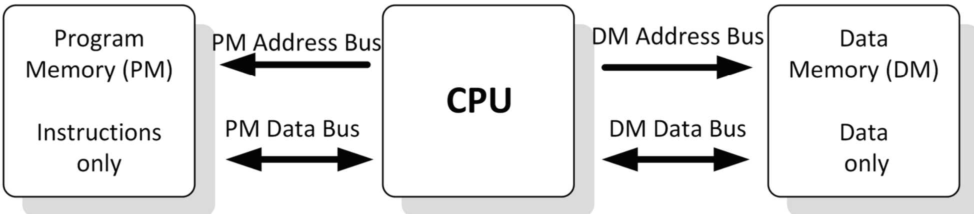

Figure 1: *Harvard processor architecture*

The DSP processor consumes most of the loop execution time in the algorithms, so it has a built-in CPU instruction cache that can store the 32 most commonly used programming instructions. This processor concept is called Super Harvard Architecture (SCHARC) (presented in Fig. 2) designed by engineers of the Analog Devices company, which unified the enhanced DSP under the name SHARC®DSP. To accelerate the information flow, they have connected it to the data memory I/O controller, which provides high-speed parallel and serial communications ports, *[5]*.

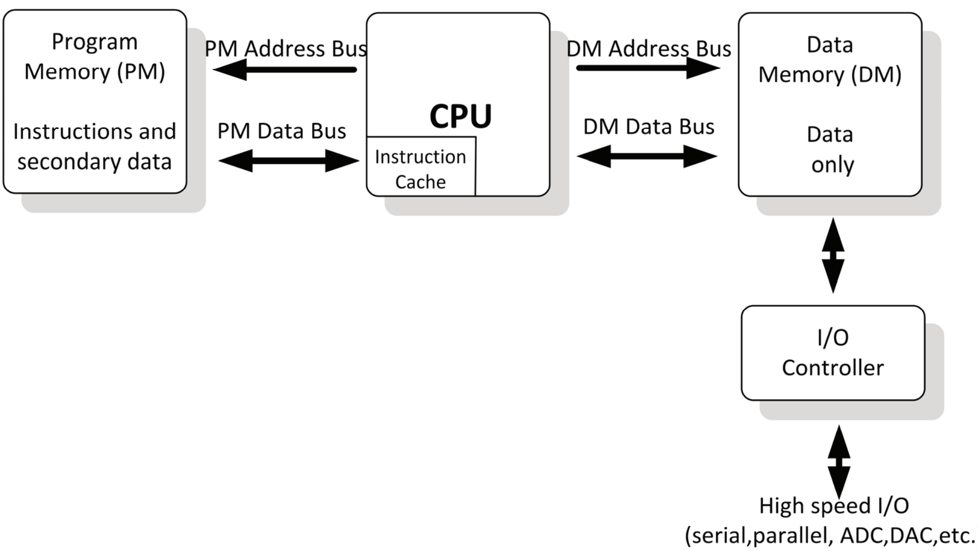

Figure 2: *Super Harvard processor architecture*

A specific feature of the Harvard architecture is the instruction overlap, i.e. instruction pipelining which allows the CPU to execute all execution steps (fetch, decode, execute) in parallel, *[6]*. The ability for instruction pipelining (presented in Fig. 3) is a significant element for achieving high processor performances in digital signal processing, *[2]*.

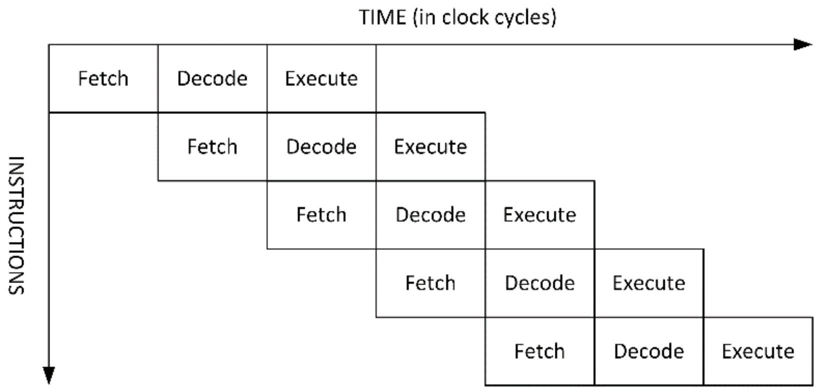

Figure 3: *Instruction pipelining*

The number of levels of parallel instruction execution differs from processor to processor: as the number of levels is higher, the performances of the processor are better, i.e. studying the parallel instruction execution leads to reduced average execution time of the instructions. Aiming to enhance the memory and speed memory access in one instruction cycle, various producers have modified the Harvard processor architecture in different ways, *[2]*.

For DSP performance improvement, two approaches of parallel processing were developed: VLIW (Very Long Instruction Word) and SIMD (Single-Input Multiple-Data). The VLIW processor architecture is suitable for numerically demanding algorithms due to embedded multiple units for the parallel execution of instructions in one cycle. More details about parallel processing can be found in *[2], [9], [10]*. The SIMD processor architecture is used in operations of big data groups, e.g. matrix operations, image processing, graphics, simulations, numerical analysis, etc., *[2]*.

3 MOST COMMONLY USED APPLICATIONS AND ALGORITHMS

It is important to consider the requirements of the applications that would be executed on the desired DSP. Dominant producers in sales and the development of the DSPs are presented in Table 1 with a list of applications and algorithms from literature:

Table 1: *An overview of DSP applications and algorithms*

Producers	**DSPs**	**APPLICATIONS AND ALGORITHMS**
Analog Devices	ADSP-21xx 16bit, fixed point; 32bit, floating and fixed point	wideband sinusoidal (WS) speech, *[11]*, Dual Tone Multi-Frequency (DTMF) signals, *[12]*; image processing and resilient propagation algorithms, *[13]*; intravascular ultrasound, *[14]*, active power filter, *[15]*; image reconstruction algorithms, *[16]*
	Blackfin	Optimization of MP3 decoder, *[17]*; audio equalizer, *[18]*, driver fatigue detection system, *[19], [20]*; fuzzy logic controller, *[21]*, guitar effectors *[22]*, H.264/AVC encoder, *[23]*, graphic equalizer, *[24]*
Lucent Technologies and AT&T	DSP16xx 16bit, fixed point; DSP32xx 32bit, floating point	multineuron recordings, *[25]* multi-channel dual-tone multiple frequency detection, *[26]*; digital lock in amplifier, *[27]*; matrix-pencil approach, *[28]*; noise cancellation, *[29]*; control of brushless DC (BLDC) drives, *[30]*
Motorola	DSP561xx 16 bit, fixed point; DSP560xx 24 bit, fixed point; DSP653xx 24 bit, fixed point; DSP96002 32 bit, floating point	Extracting signal components, *[31]*; real-time speech compression, *[32]*
	StarCore	Radix-4 FFT, *[33]*; least mean square adaptive filter algorithm, *[34]*; convolutional face finder algorithm (for teleconferencing, security access control, etc.), *[35]*
Texas Instruments	TMS320Cxx 16 bit, fixed point; TMS320Cxx 32 bit, floating point	rapid prototyping, *[36]*; acoustic OFDM transmitter, *[37]*; voltage frequency control of induction motor drive, *[38]*; LISA models, *[39]*; active noise control, *[40]*; noise reduction in speech signals, *[41]*
	TMS320LF	temperature humidity detection, *[42]*

DSP is present in all areas where the information is processed in digital form or controlled using digital processors, some of which are shown in Table 2, *[5], [43]*.

Table 2: *DSP fields of use and applications*

AREA	DSP algorithm	APPLICATION
Communication	Speech coding/decoding; speech encryption/decryption; speech recognition; speech synthesis; speaker identification; echo cancellation; data compression;	Digital mobile telephony, *[44]*; multimedia computers, secure communications; satellite phones; robotics; automotive applications; multimedia workstations; speakerphones; modems;
	Modem algorithms	Digital mobile telephony; digital audio broadcast; digital television
Consumer	Noise cancellation; audio equalization; ambient acoustics emulation; audio mixing and editing; sound synthesis	Consumer/professional audio; music; multimedia computers, *[45]*; advanced user interfaces
	Vision; image compression/decompression; image compositing	Robotics; security; multimedia computers; navigation; digital video *[46]*; digital photography; consumer video; advanced user interfaces;
Industrial, medicine and military	Image processing, beamforming	Magnetic resonance imaging (MRI)*[47]*; ultrasound, *[48]*; CT; ECG, *[49]*; process monitoring and control, *[50], [51]*; vision systems, *[52]*; navigation; radar/sonar, *[53]*; digital radio;

- Communication systems and audio application
    - Adaptive echo and noise cancellation

Application for adaptive filtering, i.e. attenuation of undesired echo in a telecommunication network, provided by modelling the echo path using an adaptive filter and subtracting the echo path output approximation, *[54]*.

- Digital mobile telephony

Digital signal processors embedded in mobile phones are used for signal and data processing (e.g. for speech coding, measuring consolidation of signals, voice mail, modulation and demodulation, etc.). Modern DSP chips are optimized for wireless communication, and they provide affordable and high-quality products, *[55], [56]*.

- Digital television

Interactivity, internet access, shopping, recording shows for watching later, etc. are just some examples of what digital television provides to consumers. DSP plays a key role in the processing, coding/decoding and modulation/demodulation of video and audio signals. For example, compressed video and audio before transfer and perfect image and voice are impossible without DSP, *[55]*.

- Digital audio adjustment of the voice

The major example of DSP application is the improvement of audio quality and its functionality. Audio adjustment of different voices is used in film, television and radio engineering to develop the sound background, *[55]*.

- Creating artificial speech

With the development of semiconductor technology and digital signal processors, artificial voices have almost assumed the voice quality of real human speech (e.g. Speak and Spell, TI, 1982.), *[55]*.

- o Speech recognition

The speech recognition system is based on a training system for the recognition, digitization, and storage of every spoken word. The recognition step is based on the search for matching words for every spoken word which is digitized and saved in the base. The problem occurs when the system cannot recognize speech, e.g. due to the insufficient breaks between words, fast speaking, unclear word pronunciation or presence of background noises. To resolve these problems, DSP has two major operations: parameter insulation (in order to create a sample, a clean pattern is chosen from spoken word) and pattern matching (pattern is compared with patterns in memory), *[55]*.

- Biomedical applications

Most modern medical applications, such as electrocardiography (ECG), digital stethoscopes, pulse oximeters, etc., require DSP processing. One of the DSP processors appropriate for that application is Texas Instruments TMS320C5515, based on fixed-point arithmetic. Texas Instruments has developed an MDK (Medical Development Kit) based on the C5515 DSP processor that supports all developing medical applications, *[57]*.

- o Electrocardiography monitoring

Electrocardiography (ECG) is a procedure for data collection about the electrophysiology of the human heart. DSP is needed to read digital signals from an analogue-to-digital converter (ADC) over a serial peripheral interface (SPI), for noise reduction and for decoupling the key features of the ECG, *[55]*.

- o Anaesthesia control

An automated closed control system with embedded DSP processor for separating signals which come from brain serves to control the anaesthetic in the patient's body and to monitor the patient's condition. DSP plays a key role in the separation of auditory evoked response (AER) from background EEG signal. AER is part of the EEG signal: a few times weaker, but a significant signal. AER is an electrical reaction of the brain to external sounds, so it is essential for a transition assessment from consciousness to unconsciousness when the patient is anaesthetized, *[55]*

- Meteorology

DSP is used for temperature control of the sensor wire at constant temperature used in wind speed measuring instruments. DSP executes extra operations such as linearizing the output voltage of anemometers and controlling the user interface directly or using a control program on a master computer, *[58]*.

4 PRACTICAL IMPLEMENTATION OF THE EVALUATION MODEL

The TMDXEVM8148 evaluation model is based on Texas Instruments processor DM814x/AM387x for developing applications sensitive to power supply, consumer, and medical video applications which require less video streaming, *[59]*. The digital media processor (DM8148) provides fast and high-quality creation of unique applications such as video security, video conferencing, navigation, advanced portable consumer electronic devices with high end gaming support, digital signage, smart home controller applications, etc. The evaluation model has two processors: master ARM Cortex-A8 processor, which goes up to 1 GHz, and slave processor TI C674x VLIW DSP which goes up to 750 MHz, *[59], [60]*.

EVM works with GStreamer, which helps in creating programs for parallel execution and creates different multimedia applications: streaming, video editing, etc. The C6Accel API allows the memory share between DSP and ARM, i.e. parallel working. Generally, it is used for easy intercommunication between the ARM and DSP. The C674x processor architecture contains a bi-level internal core, the cache memory with the support of external memory. On the first level, the memory is divided into L1P (software cache) and the L1D (data cache). If the requested information is not contained in the cache memory, it is then retrieved from the next lower program levels: L2 or external memory, *[10]*. The architecture of the cache processor C674x is shown in Fig. 4. L1PChronic and L1D are built into the SRAM cache to 32 KB. All memory and data paths are controlled by the cache memory controller, *[61]*.

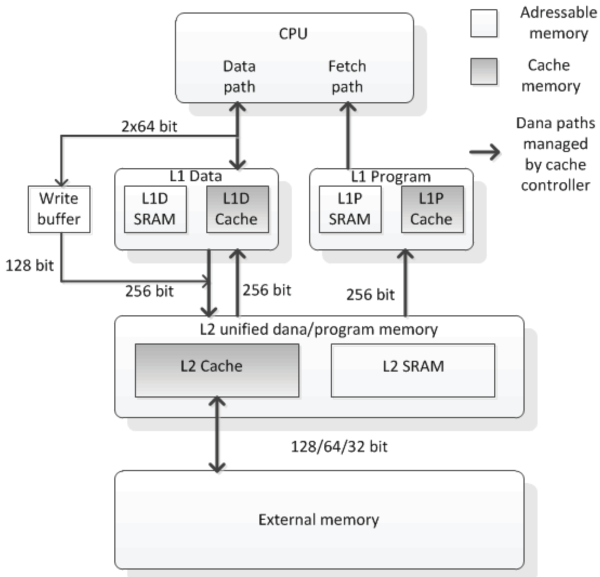

Figure 4: *Architecture of the cache processor C674x*

The registers ensure the control setting mode and control various processor operations. Interrupt Controller (INTC) is responsible for the control of the interruption in the program and management of the CPU. More details about execution time comparison can be found in, *[62]*.

Let us consider a numerical example. An executing program is given for the Monte Carlo method used in numerical integration functions executed in an integrated development environment (IDE) of the Code Composer Studio (CCSv5) supported by Texas Instruments microcontroller and embedded processors. Execution time of the loop on the digital signal processor without the level of optimization is 3.1373×10^{-306} seconds.

If the optimization level is set, the execution time of the loop of the numerical integration with the Monte Carlo method is $1.112554 \times 10^{-308}$ seconds. For comparison, the execution time of the loop of the numerical integration with the Monte Carlo method on AMD Dual-Core 2.30 GHz processor is 8.78 seconds.

The main problem for an image-and-video processing system is the time of algorithm execution. Different methods for minimization operations and memory access use a different algorithm in every loop iteration, and most of the methods for execution time minimization are based on a pipeline.
Results and execution time comparisons of the image processing from a camera in different stages are presented in Table 3. It can be concluded that the digital signal processor is a better choice for image processing in comparison with other processors regarding the execution time. More examples of execution time comparisons can be found in *[63]*.

Table 3: *Execution time for various functions using different processors*

Function	Matlab (ms)	ARM (ms)	DSP (ms)
Transform	1536	35.41	36.2
Gaussian filter	252	5.8	3.1
Horizontal interpolation	621.20	6.9	4.7
DX filter	920.3	5.4	0.2

5 DISCUSSION

Due to increasing demand for better performance of processing, there are possibilities for improving performance in clock rate, data and instruction level parallelism, decreasing the switching time of the device, etc., *[64]*. Owing to the demand for different multiple applications and the possibilities of running multiple tasks, high-performance processors have been developed. Classification of the microprocessors is presented in Figure 5.

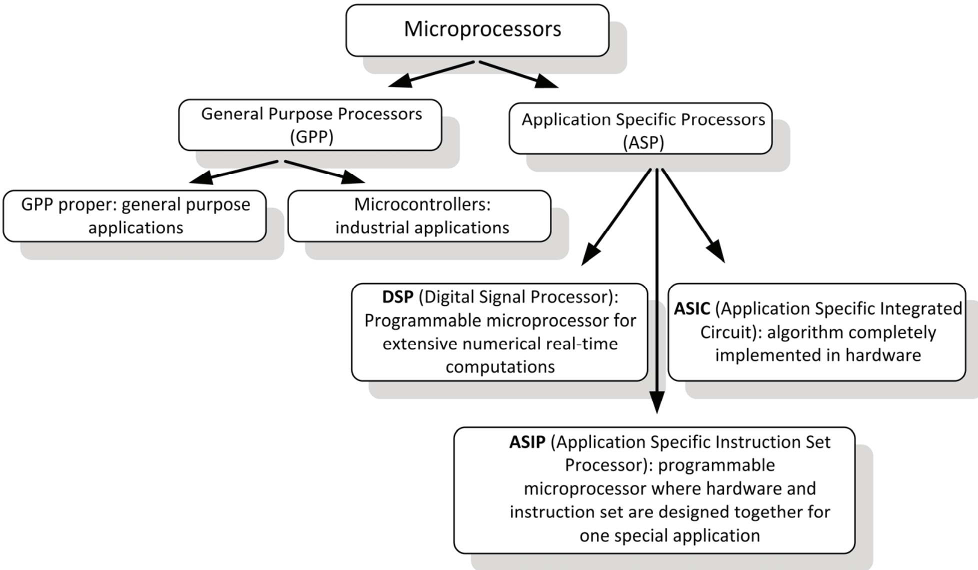

***Figure** 5: Classification of microprocessors*

General purpose processors (GPP) are used in CPUs for PCs and workstations, and have a general purpose. DSPs are microprocessors specialized for signal processing applications and embedded in mobile devices in order to optimise performance and energy consumption, *[65]*. Nowadays, multi-core processors in PCs use parallel running instructions, and are based on shared or distributed cache memory and can execute up to four instructions per cycle, while high-performance DSP can execute up to eight instructions per cycle, *[66]*. GPPs generally have Single Instruction Multiple Data (SIMD) architecture to improve their performance in data processing, *[67]*, while DSP has very long instruction word (VLIW) or SIMD operations to improve their performance, as mentioned above.

6 CONCLUSION

Digital signal processors have been undergoing massive development in the last ten years, and they are embedded in different devices (from cell phones to advanced scientific devices).

The particularity of the DSP architecture enables the development of fast and efficient applications in all areas of human activity. Due to the basic architecture of the processor regarding the data collection, data processing and transmission, the DSP achieves its maximum in millions of instructions per second. Although developers of the GPP have increased its performance, the GPP with SIMD has the ability to compute intermediate complex instructions only. Furthermore, GPP includes DSP instructions and implements DSP algorithms but it still often provides only partial solutions, *[67], [68]*.

Practical results, as described in Section 4, show the great advantages of the DSP in comparison with commonly used processors regarding the execution time of the numerical integration.

This paper gives a review of the basic architecture of DSP and the diversity of its application. Digital signal processors may be of great interest to developers who work on application development in these, or similar areas.

References:

[1] **G. Frantz**: *Signal core: A short history of the digital signal processor*, IEEE Solid-State Circuits Magazine, vol. 4, no. 2, pp. 16–20, 2012

[2] **M. E. Angoletta**: *Digital signal processor fundamentals and system design*, CAS-CERN Accelerator School: Course on Digital Signal Processing, pp. 167–229, 2007

[3] **J. Eyre, J. Bier**: *The Evolution of DSP Processors*, IEEE Signal Processing Magazine, vol. 17, no. 2, pp. 43–51, 2000

[4] **W. Kester**: *Mixed-Signal and DSP Design Techniques*. Analog Devices, Inc, 2003

[5] **S. W. Smith**: *Digital Signal Processors*, in *The Scientist and Engineer's Guide to Digital Signal Processing*, Second Edi., San Diego: California Technical Publishing, 1997, pp. 503–534

[6] **B. Paillard**: *An Introduction To Digital Signal Processors*. Génie électrique et informatique Université de Sherbrooke, 2002

[7] **D. Stranneby**: *Digital Signal Processing: DSP and Applications*. 2001

[8] **T. Ferdous**: *Design and FPGA-based implementation of a high performance 32-bit DSP processor*, Proceeding of the 15th International Conference on Computer and Information Technology, ICCIT 2012, pp. 484–489, 2012

[9] **R. Chassaing**: *DSP Applications Using C and the TMS320C6x DSK*. 2003

[10] **Texas Instruments**: *TMS320C674x DSP CPU and Instruction Set*, 2010

[11] **A. P. Q. Unisa, R. C. L. Guevara**: *Real-time implementation of wideband sinusoidal speech coder on ADSP-21065L*, in *2009 16th International Conference on Digital Signal Processing*, 2009, pp. 1–5

[12] **R. Subramaniam et al.**: *Performance of dual tone multi-frequency signal decoding algorithm using the sub-band non-uniform discrete Fourier transform on the ADSP-2192 processor*, Microprocessors and Microsystems, vol. 27, no. 10, pp. 501–510, 2003

[13] **L. M. Patnaik, K. Rajan**: *Target detection through image processing and resilient propagation algorithms*, Neurocomputing, vol. 35, pp. 123–135, 2000

[14] **S. Freear et al.**: *An intravascular ultrasound imaging system*, in *Multiprocessor DSP (Digital Signal Processing) - Applications, Algorithms and Architectures, IEE Colloquium on (Digest No.1995/116)*, 1995, p. 1/1-1/5

[15] **K. P. Sozanski**: *Harmonic compensation using the sliding DFT algorithm*, in *PESC Record - IEEE Annual Power Electronics Specialists Conference*, 2004, vol. 6, pp. 4649–4653

[16] **K. Rajan, L. M. Patnaik**: *CBP and ART image reconstruction algorithms on media and DSP processors*, Microprocessors and Microsystems, vol. 25, no. 5, pp. 233–238, 2001

[17] **B. Samuel, A. Jhunjhunwala**: *Real time implementation and optmization of MP3 decoder on DSP*, in *Canadian Conference on Electrical and Computer Engineering*, 2008, pp. 699–702

[18] **M. Gopala Krishnan**: *Audio equalizer implementation using ADSP-BF 533*, Middle - East Journal of Scientific Research, vol. 20, no. 12, pp. 2391–2394, 2014

[19] **J. Tang et al.**: *Research of driver fatigue detection system based on ADSP-BF548*, in *2010 International Conference on Mechanic Automation and Control Engineering, MACE2010*, 2010, pp. 3380–3383

[20] **J. Tang et al.**: *Design of ADSP-BF548 Fatigue Driving Detection System Based on Eye Features*, in *International Conference on Automatic Control and Artificial Intelligence (ACAI 2012)*, 2012, vol. 2012, no. 598 CP, pp. 821–824

[21] **P. Maji et al.**: *Realization of reconfigurable FLC on ADSP-BF537 processor*, in *2013 4th International Conference on Computing, Communications and Networking Technologies, ICCCNT 2013*, 2013

[22] **J. Fan et al.**: *The realization of multifunctional guitar effectors & synthesizer based on ADSP-BF533*, in *2008 11th IEEE Singapore International Conference on Communication Systems, ICCS 2008*, 2008, pp. 199–202

[23] **S. L. Yan, J. W. Sun**: *Implementation and optimization of H.264/AVC Encoder on Blackfin (ADSP-BF537) processor*, in *CIMCA 2006: International Conference on Computational Intelligence for Modelling, Control and Automation, Jointly with IAWTIC 2006: International Conference on Intelligent Agents Web Technologies ...*, 2007

[24] **A. Geetha**: *Implementation of graphic equalizer using ADSP-BF533*, Middle - East Journal of Scientific Research, vol. 19, no. 6, pp. 875–879, 2014

[25] **R. Ggdicke et al.**: *Real-time separation of multineuron recordings with a DSP32C signal processor.*, Journal of neuroscience methods, vol. 57, no. 2, pp. 187–93, 1995

[26] **S. L. Gay et al.**: *Algorithms for Multi-Channel DTMF Detection For the WE DSP32 Family*, in *ICASSP: International Conference on Acoustics, Speech, and Signal Processing*, 1989, pp. 1134–1137

[27] **J. Gaspar et al.**: *Digital lock in amplifier: Study, design and development with a digital signal processor*, Microprocessors and Microsystems, vol. 28, no. 4, pp. 157–162, 2004

[28] **T. K. Sarkar et al.**: *A Real-Time Signal Processing Technique for Approximating a Function by a Sum of Complex Exponentials Utilizing the Matrix-Pencil Approach*, Digital Signal Processing, vol. 4, no. 2, pp. 127–140, 1994

[29] **A. V. Oppenheim et al.**: *Single sensor active noise cancellation based on the EM algorithm*, in *IEEE International Conference on Acoustics, Speech, and Signal Processing*, 1992, vol. 1, pp. 277–280 vol.1

[30] **K. J. Tseng**: *DSP-based control of brushless DC drives for direct-driven robotic arms*, Microprocessors and Microsystems, vol. 19, no. 10, pp. 581–589, 1995

[31] **P. D. West, M. D. Austin**: *Extracting in-phase and quadrature signal components from a bandlimited real signal using a closed form optimal (MSE) halfband multirate filter design and its implementation on the Motorola DSP56001/DSP56ADC16*, in *[Proceedings] ICASSP-92: 1992 IEEE International Conference on Acoustics, Speech, and Signal Processing*, 1992, vol. 4, pp. 685–688 vol.4

[32] **T. Srikanthan et al.**: *An OLE-based speech compression system for multimedia applications*, Microprocessors and Microsystems, vol. 22, no. 1, pp. 41–48, Jun. 1998

[33] **E. Ben Zeev et al.**: *Efficient radix-4 FFT on StarCore SC3000 DSPs*, *EE Times Automotive DesignLines*, pp. 1–8, 2007

[34] **W. T. Padgett**: *Efficient parallel implementation of the LMS algorithm on a multi-ALU architecture*, 2002 IEEE International Conference on Acoustics, Speech, and Signal Processing, vol. 4, p. IV-3928-IV-3931, 2002

[35] **S. Roux et al.**: *Embedded convolutional face finder*, in *2006 IEEE International Conference on Multimedia and Expo, ICME 2006 - Proceedings*, 2006, vol. 2006, pp. 285–288

[36] **K. H. Hong et al.**: *Rapid prototyping of DSP algorithms on VLIW TMS320C6701 DSP*, Microprocessors and Microsystems, vol. 26, no. 7, pp. 311–324, 2002

[37] **H. Yan et al.**: *DSP implementation of SISO and MIMO OFDM acoustic modems*, in *OCEANS'10 IEEE Sydney, OCEANSSYD 2010*, 2010

[38] **C. S. Kamble et al.**: *Digital Signal Processor Based V/f Controlled Induction Motor Drive*, 2010 3rd International Conference on Emerging Trends in Engineering and Technology, pp. 345–349, 2010

[39] **S. Pees et al.**: *LISA-machine description language for cycle-accurate models of programmable DSP architectures*, Proceedings 1999 Design Automation Conference Cat No 99CH36361. pp. 933–938, 1999

[40] **A. K. Wang, B. Tse**: *Adaptive active noise control for headphones using the TMS320C30 DSP*, 1997

[41] **M. Romanin et al.**: *A spectral subtraction rule for real-time {DSP} implementation of noise reduction in speech signals*, Proc. Digital Audio Effects (DAFx-10), no. 6, pp. 1–5, 2009

[42] **W. hao, S. sha**: *Based on TMS320LF2407 Environment Temperature Humidity Detection*, Physics Procedia, vol. 25, pp. 1258–1263, 2012

[43] **P. Lapsley et al.**: *DSP processor fundamentals : architectures and features*. IEEE Press, 1997

[44] **A. Gatherer et al.**: *DSP-based architectures for mobile communications: Past, present and future*, IEEE Communications Magazine, vol. 38, no. 1, pp. 84–90, 2000

[45] **Y. Zhang et al.**: *ASIP Approach for Multimedia Applications Based on a Scalable VLIW DSP Architecture*, Tsinghua Science and Technology, vol. 14, no. 1, pp. 126–132, 2009

[46] **M. Hosemann et al.**: *Implementing a Receiver for Terrestrial Digital Video Broadcasting in Software on an Application-Specific DSP*, in *IEEE Workshop onSignal Processing Systems, 2004. SIPS 2004.*, 2004, pp. 53–58

[47] **W. Tang, W. Wang**: *A low-cost multichannel spectrometer for magnetic resonance imaging*, in *5th International Conference on Bioinformatics and Biomedical Engineering, iCBBE 2011*, 2011

[48] **F. K. Schneider et al.**: *A fully programmable computing architecture for medical ultrasound machines*, IEEE Transactions on Information Technology in Biomedicine, vol. 14, no. 2, pp. 538–540, 2010

[49] **K. Mankodiya et al.**: *Portable electrophysiologic monitoring based on the OMAP-family processor from a beginners' prospective*, in *DSP 2009: 16th International Conference on Digital Signal Processing, Proceedings*, 2009

[50] **a. R. Bin Abdullah, a. Z. Bin Sha'ameri**: *Real-Time Power Quality Monitoring System Based On TMS320CV5416 DSP Processor*, 2005 International Conference on Power Electronics and Drives Systems, vol. 2, pp. 1668–1672, 2005

[51] **K. V. Kumar et al.**: *Condition monitoring of DSP based online induction motor external fault detection using TMS320LF2407 DSP*, in *Proceedings of 2011 International Conference on Process Automation, Control and Computing, PACC 2011*, 2011

[52] **X. T. Nguyen et al.**: *A real-time DSP-based hand gesture recognition system*, in *2012 IEEE International Symposium on Signal Processing and Information Technology, ISSPIT 2012*, 2012, pp. 286–291

[53] **A. Heale, L. Kleeman**: *A real time DSP sonar echo processor*, Proceedings. 2000 IEEE/RSJ International Conference on Intelligent Robots and Systems (IROS 2000) (Cat. No.00CH37113), vol. 2, pp. 1261–1266, 2000

[54] **S. M. (Sen-M. Kuo et al.**: *Real-time digital signal processing fundamentals, implementations and applications*

[55] **E. C. Ifeachor, B. W. Jervis**: *Digital Signal Processing A Practical Approach*, 2nd ed. Prentice Hall, 2002

[56] **B. D. de Dinechin et al.**: *DSP-MCU processor optimization for portable applications*, Microelectronic Engineering, vol. 54, no. 1–2, pp. 123–132, 2000

[57] **V. Markandey**: *ECG Implementation on the TMS320C5515 DSP Medical Development Kit (MDK)*, 2010

[58] **R. Steinhilber, P. M. Wagner**: *A digital signal processor for anemometer control*, Experiments in Fluids, vol. 17, pp. 302–306, 1994

[59] **Texas Instruments**: *TMS320DM814x DaVinci ™ Digital Media Processors*, 2011

[60] **Texas Instruments**: *TMDXEVM8148 Evaluation Module*, 2011

[61] **Texas Instruments**: *TMS320C674x DSP Cache, User' s Guide*, Dallas, Texas, 2009

[62] **Texas Instruments**: *TMS320C674x DSP Megamodule Reference Guide*, Dallas, Texas, 2010

[63] **J. Fité Sànchez**: *Migration of a stereoscopic camera system from Matlab to the TMS320DM814x DaVinci platform*. Universitat Politècnica de Catalunya, 2012

[64] **A. Jameel et al.**: *Multiprocessors and Cache Memory*, in *Fuzzy Logic Based Power Efficient Real-Time Multi-Core System*, Springer Briefs in Applied Sciences and Technology, 2017, pp. 11–25

[65] **Y. Benmoussa et al.**: *GPP vs DSP: A performance/energy characterization and evaluation of video decoding*, Proceedings - IEEE Computer Society's Annual International Symposium on Modeling, Analysis, and Simulation of Computer and Telecommunications Systems, MASCOTS, pp. 273–282, 2013

[66] **K. Williston**: *Microprocessors vs . DSPs : Fundamentals and Distinctions*, *Berkeley Design Technology, Embedded Systems Conference, San Francisco, CA*, 2005. [Online]. Available: http://www.bdti.com/MyBDTI/pubs/050307ESC_MPUs_vs_DSPs.pdf. [Accessed: 15-Dec-2016]

[67] **He Zhiqiang et al.**: *Analysis for singal processing development with general purpose processor*, in *7th International Conference on Communications and Networking in China*, 2012, pp. 792–796

[68] **M. Elkhatib, S. Olafsson**: *Optimizing efficiency and flexibility in DSP systems*, *EDN Network*, 2013. [Online]. Available: http://www.edn.com/design/systems-design/4404886/Optimizing-efficiency-and-flexibility-in-DSP-systems. [Accessed: 15-Dec-2016]